

# REDUNDANT INTERCONNECT HIGH CURRENT BIPOLAR DEVICE AND METHOD OF FORMING THE DEVICE

## BACKGROUND OF THE INVENTION

### Technical Field

5           The present invention relates generally to integrated circuits, and more particularly, to a bipolar transistor having the capacity to accommodate higher current while maintaining a small foot print.

### Related Art

10           In order to increase the current capacity of a bipolar NPN transistor, the size of the emitter contact is increased. However, conventional methods of increasing the size of the emitter contact also result in an increased device foot print, or overall size. As the trend toward smaller and smaller devices  
15 continues in the industry, it is desirable to produce a bipolar NPN transistor having an increased current capacity while maintaining a small foot print.

## SUMMARY OF THE INVENTION

20           A first general aspect of the present invention provides a bipolar transistor, comprising: a base; a base contact formed

within the base; and an emitter contact formed within the base, wherein the emitter contact surrounds the base contact.

A second general aspect of the present invention provides a device, comprising: a base; a base contact formed within the base; and an emitter contact formed within the base, wherein the emitter contact extends around at least two sides of the base contact.

A third general aspect of the present invention provides a bipolar transistor, comprising: a base; an emitter contact formed within the base; a base contact formed within the base; and a first wiring stack formed atop the emitter contact and a second wiring stack formed atop the base contact, wherein the second wiring stack includes at least one more wiring level than the first wiring stack.

A fourth general aspect of the present invention provides a device, comprising: at least two bipolar transistors, wherein each bipolar transistor further comprises: a base contact; an emitter contact surrounding the base contact; and wherein at least one side of the emitter contact of the at least two bipolar transistors are in electrical contact.

A fifth general aspect of the present invention provides a device, comprising: at least two bipolar transistors, wherein the bipolar transistors are electrically connected to one another,

and wherein a first bipolar transistor has a first wiring stack  
and a second bipolar transistor has a second wiring stack,  
wherein the second wiring stack comprises at least one more  
wiring level than the first wiring stack.

5       The foregoing and other features of the invention will be  
apparent from the following more particular description of the  
embodiments of the invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

10       The embodiments of this invention will be described in  
detail, with reference to the following figures, wherein like  
designations denote like elements, and wherein:

Fig. 1A depicts a top view of a related art bipolar NPN  
transistor;

15       Fig. 1B depicts a cross-sectional view of the related art  
bipolar NPN transistor of Fig. 1A;

Fig. 2A depicts a top view of a bipolar NPN transistor in  
accordance with a first embodiment of the present invention;

20       Fig. 2B depicts a cross-sectional view of the transistor of  
Fig. 2A in accordance with a first embodiment of the present  
invention;

Fig. 3A depicts a top view of the transistor of Fig. 2A  
having stacked wiring connected thereto in accordance with a

second embodiment of the present invention;

Fig. 3B depicts a cross-section view of the transistor of Fig. 3A in accordance with a second embodiment of the present invention;

5 Fig. 4A depicts a cross-sectional view of the transistor of Fig. 3A in accordance with a third embodiment of the present invention;

10 Fig. 4B depicts a cross-sectional view of the transistor of Fig. 4A in accordance with a third embodiment of the present invention;

Fig. 5 depicts a top view of a grid device in accordance with a fourth embodiment of the present invention; and

15 Fig. 6 depicts a cross-sectional view of transistor wiring stacks having variable wiring levels in accordance with a fifth embodiment of the present invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Although certain embodiments of the present invention will be shown and described in detail, it should be understood that  
20 various changes and modifications may be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the

relative arrangement thereof, etc. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

Referring to the drawings, Fig. 1A shows a top view of a related art bipolar NPN transistor 10. Fig. 1B shows a cross-sectional view of the transistor 10 of Fig. 1A taken along line 1B. In the alternative, the transistor may be a PNP transistor, or other similar device. The transistor 10 comprises an isolation trench 11, a P+ substrate 12, an N+ subcollector 14, an N- collector 16 and a P+ base collector 18. The transistor 10 further includes a collector contact 20 formed within the N+ subcollector 14. Within the P+ base collector 18, an emitter contact 22 and a pair of base contacts 24 are formed.

In order to increase the amount of current the transistor 10 can safely accommodate, the emitter contact 22 is typically lengthened in the direction of the x-axis. However, lengthening the emitter contact 22 necessitates the enlargement of the base collector 18, and the entire transistor 10, which in turn adds parasitic capacitance to the various nodes of the device. This tends to slow the functioning of the overall device because the device now has to drive a higher base-collector capacitance, collector-substrate capacitance, and so on.

Therefore, it is desirable to increase the size of the

emitter contact, while maintaining a small overall device size. Accordingly, a first embodiment of the present invention provides a device or bipolar NPN transistor 100 having a large emitter contact area, while minimizing the ratio of the emitter contact area to the base collector area, as illustrated in Figs. 2A and 2B, (wherein Fig. 2A is a top view of the transistor 100 and Fig. 2B is a cross-sectional view of the transistor 100 taken along line 2B).

The transistor 100 comprises an isolation trench 111, a P+ substrate 112, an N+ subcollector 114, an N- collector 116 and a P+ base collector 118. The transistor 100 further includes a collector contact 120 formed within the N+ subcollector 114. Within the P+ base collector 118, an emitter contact 122 and a base contact 124 are formed. The base contact 124 is a point contact, and the emitter contact 122 forms a ring around the base contact 124. By providing the emitter contact 122 in the form of a ring surrounding the base contact 124, the size of the emitter contact 122 is enlarged, thereby allowing the transistor 100 to accommodate a higher current, while maintaining a low emitter contact 122 area to base collector 118 area ratio.

Because the area of the P+ base collector 118 is kept to a minimum, the P-N junction 117 between the P+ base collector 118 and the N- collector 116 is likewise minimized. Capacitance is

lowered as the area of the P-N junction 117 is lowered.

Therefore, by making the P+ base collector 118 to N- collector 116 P-N junction 117 as small as possible the transistor 100 exhibits a low base capacitance, which tends to enhance the switching speed of the transistor 100.

Next, the base contact 124, the emitter contact 122 and the collector contact 120 of the transistor 100 are wired in order for current to flow from the transistor 100 to adjacent devices and/or the outside world. The amount of current a wire can safely carry from a contact to another device is determined by the size of the wire. As the amount of current being transmitted from the transistor increases, so too must the size of the wires increase.

Conventionally, this needed increase in wire size was accomplished by increasing the width of the wires (in the direction of the y-axis). This, however, defeats the purpose of the first embodiment of the present invention, namely, producing a transistor capable of carrying a high current while maintaining a small overall device size. If the width of the wires was increased to accommodate the higher current therethrough, the base contact 124 and the emitter contact 122 would have to be spread further apart to make room for the wider wires. This would necessitate an increase in the overall size of the

transistor 100.

Moreover, utilizing wires that are too small to safely carry the higher currents may result in a phenomenon referred to as "electromigration." In particular, the particles that make up the wire are pulled in the direction of current flow. This results in the displacement of wire particles along the length of the wire, such that voids are created upstream and the wire becomes thicker downstream of the current flow. As a result, the wire is susceptible to failure.

Accordingly, a second embodiment of the present invention provides a method of wiring the transistor 100 that safely accommodates a higher current flow, and reduces the electromigration problem. In particular, Fig. 3A shows a top view of the transistor 100 of Figs. 2A and 2B having wires extending from the base contact 124, the emitter contact 122 and the collector contact 120, and Fig. 3B shows a cross-sectional view of Fig. 3A taken along line 3B.

As illustrated, the wiring forms a vertical stack atop each contact 124, 122, 120, in order to increase the size (in this case the thickness in the direction of the z-axis) of the wires without increasing the overall foot print of the transistor 100. For example, the collector contact 120 has a collector contact stack 121 thereover, comprising a contact 128a, a first wiring



level 132a, a via 136a, and a second wiring level 140a. The emitter contact 122 has an emitter contact stack 123 formed thereover, comprising a contact 128b, and a first wiring level 132b. Likewise, the base contact 124 has a base contact stack 125, comprising a contact 128c, a first wiring level 132c, a via 136c, and a second wiring level 140c.

The stacks 121, 123, 125, are typically formed using known damascene techniques. Specifically, a first dielectric layer 126, such as oxide,  $\text{SiO}_2$ , silicon nitride, polyimides, etc., is deposited over the surface of the transistor 100, using conventional deposition techniques. Holes are then etched, using known techniques, within the first dielectric layer 126 atop the collector, emitter and base contacts 120, 122, 124. A conductive material, such as tungsten or other similar material, is deposited over the first dielectric layer 126 to fill the holes formed therein. The surface of the first dielectric layer 126 is then planarized, using chemical-mechanical polishing (CMP), or other similar technique, to form contacts 128a, 128b, 128c.

A second dielectric layer 130 is then deposited over the first dielectric layer 126 and the contacts 128a-c. Holes are etched within the second dielectric layer 130 over each contact 128a-c. A conductive material, such as aluminum, copper, or other similar material, is deposited over the second dielectric

layer 130 to fill the holes formed therein. The surface of the second dielectric layer 130 is then planarized to form a first wiring level 132a, 132b, 132c of each individual stack 121, 123, 125.

5        A third dielectric layer 134 is deposited over the second dielectric layer 130 and the first wiring level 132a-c. Holes are etched within the third dielectric layer 134 over the first wiring level 132a, 132c, of the collector contact 120 and the base contact 124, respectively. A conductive material, such as tungsten or other similar material, is deposited over the third dielectric layer 134 to fill the holes formed therein. The surface of the third dielectric layer 134 is then planarized to form vias 136a and 136c therein.

15       A fourth dielectric layer 138 is deposited over the third dielectric layer 134 and the vias 136a and 136c. Holes are etched within the fourth dielectric layer 138 over the vias 136a, 136c. A conductive material, such as aluminum, copper, or other similar material, is deposited over the fourth dielectric layer 138 to fill the holes formed therein. The surface of the fourth dielectric layer 138 is then planarized to form a second wiring level 140a and 140c for the collector contact stack 121 and the base contact stack 125 therein.

20       The wiring stacks 121, 123, 125 provide the transistor 100

with an increased current capacity without the typical electromigration problems described above, namely because of the increased wire thickness in the z direction. This is particularly true for the emitter contact stack 123 because the emitter contact 122 typically exhibits the greatest electromigration problems due to the high current passing therethrough. In fact, the second wiring level 140c of the base contact stack 125 is referred to as a "redundant contact" because the second wiring level 140 is only needed to raise the base contact 124 above the emitter contact 122 wiring (in this example, the first wiring level 132). The current running through the base contact 124 is much lower than that of the emitter contact 122, therefore, the base contact 124 has few problems with electromigration, and has little need for the added wiring thickness produced by the vertical stacks. However, because the emitter contact 122, and the wiring connected thereto, forms a ring around the base contact 124, the additional wiring level is needed to allow the base contact 124 to extend above the emitter contact stack 123 and make connection with an adjacent device.

Figs. 4A and 4B illustrate a third embodiment, wherein additional wiring levels may be formed for devices needing to accommodate an even higher current. Fig. 4A shows a top view of

the transistor 100 having three wiring levels, rather than just two wiring levels, and Fig. 4B shows a cross-sectional view of Fig. 4A taken along line 4B. In contrast to the transistor 100 illustrated in Fig. 3B, the transistor 100 in Fig. 4B has vias 136a, 136b, 136c formed within the third dielectric layer 134 above each contact 128a-c, rather than just above the contacts 128a, 128c of the collector and base contacts 120, 124.

Likewise, the second wiring level 140a-c is formed within the fourth dielectric layer 138 above each contact 128a-c, rather than just over the contacts 128a, 128c of the collector and base contacts 120, 124.

Thereafter, a fifth dielectric layer 142 is deposited over the fourth dielectric layer 138 and the second wiring layer 140a-c, using known techniques. Holes are etched within the fifth dielectric layer 142 above the collector contact 120 and the base contact 124. A conductive material, such as tungsten, or other similar material, is deposited over the fifth dielectric layer 142 to fill the holes formed therein. The surface of the fifth dielectric layer 142 is then planarized to form second vias 146a and 146c therein.

A sixth dielectric layer 148 is then deposited, using known techniques, over the fifth dielectric layer 142 and the second vias 146a and 146c. Holes are etched within the sixth dielectric

layer 148 above the second vias 146a and 146c. A conductive material, such as aluminum, copper, or other similar material, is deposited over the sixth dielectric layer 148 to fill the holes formed therein. The surface of the sixth dielectric layer 148 is then planarized to form a third wiring level 150a and 150c of the collector contact stack 121 and the base contact stack 125.

As mentioned above, due to the increased wire thickness in the z direction of the wiring stacks 121, 123, 125, the transistor 100 can accommodate an increased current without the typical electromigration problems, and the additional wiring level used to connect the base contact 124 to an adjacent device, (in the previous example, the second wiring level 140c, and in this example, the third wiring level 150c), is referred to as a redundant contact.

It should be noted that the via 136b above the emitter contact 122, (Fig. 4), may be formed of a single continuous via 136b that covers the entire emitter contact 122 ring. In the alternative, the via 136b above the emitter contact 122 may be formed of individual vias. For instance, some via formation techniques limit the size of vias formed to 1 micron x 1 micron, or 0.8 microns x 0.8 microns, etc. If such a technique were used the emitter contact via 136b may be formed of a plurality of adjacently placed individual vias.

It should also be noted that the contacts 128a-c and the  
vias 136a-c, 146a,c (over all the contacts 124, 122, 120), add to  
the total thickness of the wiring. In other words, the wiring  
stacks 121, 123, 125 are even thicker because the contacts 128  
and the vias 136, 146 that connect the contacts 120, 122, 124 to  
the respective wiring levels also comprise conductive material  
that carries current therethrough.

In accordance with a fourth embodiment of the present  
invention, a "grid" device 160 may be formed by placing or  
abutting at least two or more transistors 100 together. For  
example, Fig. 5 illustrates a top view of a grid device 160  
having 24 transistors 100 connected together. The wiring levels  
are removed for ease of viewing. In particular, the ring emitter  
contact 124 of each transistor 100 shares one side of the emitter  
contact 124 with each adjacent transistor 100 it contacts or  
abuts. As a result, the current capacity of the overall device  
160 almost doubles with the addition of the first transistor 100,  
and so on with the addition of each transistor 100. (The current  
capacity is some value less than two times the current capacity  
of a single transistor 100 because the emitter contact 124 of the  
first and second transistors 100 share one side, and so on with  
each additional transistor 100.)

The wiring extending from one side of the grid device 160 is

used for current input into the device 160. Since all the transistors 100 are tied together in series, the current tends to drop as it travels from the near side 162 of the device 160 to the far side 164 of the device 160. Ideally, it is desirable to have the emitter contact 122 of every transistor 100 exposed to an equal amount of current.

Therefore, in accordance with a fourth embodiment of the present invention, the grid device 160 may be "de-biased" by adding more resistance to the near side 162 of the device 160 and progressively less resistance toward to the far side 164 of the device 160. This effectively equalizes the amount of resistance across the device 160, such that each emitter contact 124 within the device handles an approximately equal amount of current.

This is accomplished in accordance with a fifth embodiment of the present invention by utilizing transistors having various stacked wiring levels. For instance, as illustrated in Fig. 6 which shows the wiring levels of the device 160, the row of transistor 100 located at the near side 162 of the device 160 have two wiring levels 132, 140 (as illustrated in Figs. 3A and 3B), the next row of transistors 100 have three wiring levels 132, 140, 150 (as illustrated in Figs. 4A and 4B), the next row of transistors 100 have four wiring levels, and so on until the far side 164 of the device 160 is reached. This is effective

because the thinner the metal wire, the more resistance therein,  
and conversely the thicker the metal wire, the less resistance  
therein.

It should be noted that the grid device 160 illustrated in  
5 Fig. 5 is intended only as an example, and is not intended to  
limit the present in any manner. For instance, the grid device  
160 may comprise any number of transistors 100 and may be  
arranged in a variety of shapes, i.e., in the form of a T, a  
rectangle, a ring, etc. Similarly, the de-biasing embodiment  
10 illustrated in Fig. 6 is intended as an example only. The wiring  
stack could alternatively increase from a first corner of the  
device 160 to an opposing corner of the device 160, etc.  
Similarly, the number wiring levels within each wiring stack may  
be varied as desired and needed.

15 While this invention has been described in conjunction with  
the specific embodiments outlined above, it is evident that many  
alternatives, modifications and variations will be apparent to  
those skilled in the art. Accordingly, the embodiments of the  
invention as set forth above are intended to be illustrative, not  
20 limiting. Various changes may be made without departing from the  
spirit and scope of the invention as defined in the following  
claims.